



Surface Quality Optimisation of Monocrystalline and Polycrystalline Silicon Wafers through Cleaning, Etching and Texturisation Processes for Si Solar Cell Applications

Nurfarizza Surhada Mohd Nasir,¹ Ahmad Rujhan Mohd Rais,^{2*} Nurul Aqidah Mohd Sinin³ and Kamaruzzaman Sopian⁴

¹Petronas Research Sdn Bhd, Lot 3288 & 3289, Off Jalan Ayer Itam, Kawasan Institusi Bangi, 43600 Kajang, Selangor, Malaysia

²School of Physics, Universiti Sains Malaysia, 11800 USM, Pulau Pinang, Malaysia

³Solar Energy Research Institute, Universiti Kebangsaan Malaysia, 43600 Bangi, Malaysia

⁴Department of Mechanical Engineering, Universiti Teknologi PETRONAS, 32610 Seri Iskandar, Perak, Malaysia

*Corresponding author: rujhanrais@usm.my

Published online: 29 August 2025

To cite this article: Mohd Nasir, N. S. et al. (2025). Surface quality optimisation of monocrystalline and polycrystalline silicon wafers through cleaning, etching and texturisation processes for Si solar cell applications. *J. Phys. Sci.*, 36(2), 39–59. <https://doi.org/10.21315/jps2025.36.2.3>

To link this article: <https://doi.org/10.21315/jps2025.36.2.3>

ABSTRACT: Silicon (Si) wafers, critical substrates for semiconductor and photovoltaic (PV) device fabrication, require surface cleaning and damage removal to ensure high-quality performance. This study investigates the surface morphology and contamination levels of monocrystalline silicon (c-Si) and multicrystalline silicon (mc-Si) wafers before and after cleaning. Scanning electron microscopy (SEM) and Energy-dispersive X-ray (EDX) analysis revealed that, before cleaning, both wafer types exhibit micro-roughness and contain contaminants such as iron (Fe), oxygen (O), nitrogen (N), carbon (C) and fluorine (F). For the as-cut c-Si wafer, EDX data reveals a Si content of 85.08%, with contamination levels of C (9.38%), O (2.41%), N (1.45%) and F (0.68%). In mc-Si wafers, slicing introduces surface roughness and leaves residues, with the surface characterised by particulates and metallic contaminants. Following the damage removal process using nitric acid/hydrofluoric acid (HNO₃/HF) etching, the contamination levels on mc-Si wafers reduce significantly, with Si content increasing to 90.8%. In comparison, C decreases to 7.5%, and O drops to 1.7%. The wet-chemical etching removes ~5 µm–12 µm of wafer thickness, effectively eliminating surface defects and contaminants. The cleaning process reduces particulate contamination by over 90%, and a smooth, defect-free surface is observed in SEM images post-cleaning. These results demonstrate that adequate cleaning and damage removal are essential for improving solar cell efficiency by enhancing carrier lifetime, reducing surface recombination, and minimising leakage currents.

Keywords: etching, monocrystalline, polycrystalline, silicon, texturisation

1. INTRODUCTION

Silicon (Si) wafers are the foundational material for most semiconductor devices, forming the basis for various electronic components, from simple diodes to complex integrated circuits. Notably, the performance and reliability of these devices are critically dependent on the quality of the Si wafer surface, which must be meticulously controlled and maintained throughout the manufacturing process. As such, any imperfections or contaminants on the wafer surface can lead to defects in the final product, impacting yield and device functionality.

One key stage in semiconductor fabrication is preparing the Si wafer surface through a series of cleaning and etching processes. These processes are designed to remove contaminants, native oxides and residual material from previous processing steps and create an optimal surface for subsequent device fabrication stages. Furthermore, cleaning processes are critical in manufacturing monocrystalline (c-Si) and multicrystalline (mc-Si) solar cells since contamination on the Si wafer surface can negatively impact solar cell performance. These contaminants can include organic residues, particles, metallic impurities and chemical residues from earlier processing steps.¹⁻⁶ Thus, effective cleaning ensures that the wafer surface is free from contaminants, allowing for optimal electrical and optical properties and directly influencing solar cells' efficiency and reliability. After cleaning, the front surface of Si wafers will be smooth and planar without any additional surface texturisation. Unlike textured surfaces, planar Si solar cells reflect most incident photons instead of absorbing them inside.⁷

Thus, post-etching after cleaning is crucial to reduce optical losses by creating additional texture structures on the Si wafers. Note that optical losses in both c-Si and mc-Si solar cells significantly affect overall cell efficiency. These losses occur due to the reflection and transmission of light, as well as the absorption of light in non-active layers or materials. In particular, Si has a relatively high refractive index (~3.5), meaning a significant amount of light reflects from its surface.⁸⁻¹² Without surface treatment, up to 30% of the light can be lost to reflection.^{13,14} Table 1 summarises the common losses of Si wafers.

Table 1: Type of losses on c-Si and mc-Si^{7,14-18}

Type of losses	c-Si	mc-Si
Reflection losses	Lower due to uniform, effective texturing	Higher due to non-uniform texturing
Absorption losses	Losses mainly in UV	Similar to c-Si
Transmission losses	This can be minimised with thin wafers	Slightly higher due to thicker wafers needed
Scattering losses	Negligible due to single crystal structure	Higher due to grain boundaries and imperfections

Thus, texturing the surface of c-Si and mc-Si silicon is critical in fabrication. It plays a crucial role in enhancing the efficiency of solar cells by improving light absorption, reducing reflection losses, and enhancing the overall optical properties of the cell. However, the texturing process varies for c-Si and mc-Si due to their distinct crystallographic structures, and each requires tailored techniques to achieve optimal performance. A significant portion of incident light on a planar, un-textured Si surface is reflected, which reduces the amount of light available for conversion into photo-electricity. In addition, texturing dramatically reduces reflection losses by altering the surface morphology to trap light. In c-Si cells, reflection losses can be reduced from 30% to around 10%,^{19–24} while mc-Si texturing reduces reflectance to around 10%–20%.^{25–31}

Other than that, textured surfaces increase the optical path length of light within the Si wafer. When light hits the textured surface, it bounces around multiple times, increasing the probability of absorption. This is especially important for near-infrared light, which has longer wavelengths and is less efficiently absorbed. Notably, the more light absorbed, the more charge carriers are generated, leading to higher current and efficiency. The primary goal of texturing is to improve light absorption, which directly translates to better performance in terms of the solar cell's conversion efficiency. As such, textured cells exhibit higher short-circuit current density (J_{sc}) and improved overall efficiency compared to un-textured cells. In c-Si cells, the most commonly used texturing process is alkaline texturing with potassium hydroxide (KOH) or sodium hydroxide (NaOH). The etching solution preferentially etches the [100] crystallographic plane while leaving the [111] planes intact. Unlike c-Si, mc-Si cannot be textured with alkaline solutions due to its random crystallographic orientation. Instead, an acidic solution, typically a mixture of hydrofluoric acid (HF) and nitric acid (HNO₃), is used for isotropic texturing. However, this article highlights the impact of the cleaning process on Si wafers and alkaline texturing on c-Si and mc-Si on enhancing surface roughness where incident light is trapped.

1.1 Methodology

To achieve optimal efficiency in solar cell manufacturing, enhancing both the front and rear surfaces of Si wafers is essential. The cleaning process, a critical initial step in solar cell production, is pivotal in this optimisation. This process involves using various etchant solutions, which are key to ensuring the desired surface quality and higher efficiency. The Si etching process is primarily governed by two factors: (1) the surface reaction kinetics and (2) the diffusion rate of reactants to the wafer surface. These two mechanisms collectively dictate the overall rate of microstructural growth during etching, making them fundamental to controlling surface morphology and improving wafer performance for solar applications.

The Radio Corporation of America (RCA) cleaning process, originally developed by the RCA and refined by our research team, is employed to effectively clean Si wafers. This process consists of two critical steps. The first step utilises the RCA-1 solution, a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionised water (H_2O) with a volume ratio of 1:1:5 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$). The solution is heated to a temperature of 70°C – 80°C for less than 1 min to efficiently remove organic contaminants from the Si wafer surface. Following this, the wafers are subjected to the RCA-2 cleaning solution, comprising a 1:1:6 ($\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) volume ratio of hydrochloric acid (HCl), H_2O_2 and H_2O . The solution is heated to 80°C , and the wafers are immersed for 10 min, effectively eliminating metallic impurities. This meticulous cleaning procedure ensures the removal of organic and metallic contaminants, providing a clean and contaminant-free surface essential for optimising subsequent processes in solar cell fabrication.

All the work presented here was conducted on $(10 \times 10) \text{ cm}^2$ wafer size, p-type [100] c-Si and [100] mc-Si wafer. The following process was cleaning with saw damage removal solution by etching the wafers in 10% NaOH solution at 70°C for 10 min. Subsequently, the wafer is rinsed with H_2O , and the native oxide is removed from the dilute HF to form hydrophobic surfaces. Next, the texturing occurs in the solution of KOH mixed with isopropyl alcohol (IPA) and H_2O at volume ratio of 1.5:5:125 (KOH:IPA: H_2O) at 70°C for 30 min. Prior to emitter deposition, the textured wafer is cleaned in $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ with volume ratio of 1:1:5 solution at 70°C for 10 min to form hydrophilic surfaces. Finally, all the samples are rinsed with H_2O and dried with nitrogen gas ambient to ensure they are clean for visualisation and characterisation as shown in Figure 1. The method used in Srivastava et al. mainly focused on n-type [100] Si wafers cleaned by using ultrasonication for each Si wafers with area of $3.5 \times 3.5 \text{ cm}^2$ followed by texturisation process by using 2% KOH and 20% IPA solution at $80 \pm 5^\circ\text{C}$ for 15 min–90 min.¹² In this article, p-type [100] c-Si and [100] mc-Si wafer with the size of $10 \times 10 \text{ cm}^2$ was cleaned in a single cleaning process at a maximum quantity of 25 samples in one process as shown in Figure 1.³² According to Figure 1, the flowchart illustrates the step-by-step process of cleaning and texturing a $10 \times 10 \text{ cm}^2$ p-type [100] c-Si and mc-Si [100] wafer before visualisation and characterisation. As compared with Srivastava et al., the cleaning process by ultrasonication process can only be conducted only one sample at the same time.³² Thus, requires more additional preparation steps just for the cleaning process.

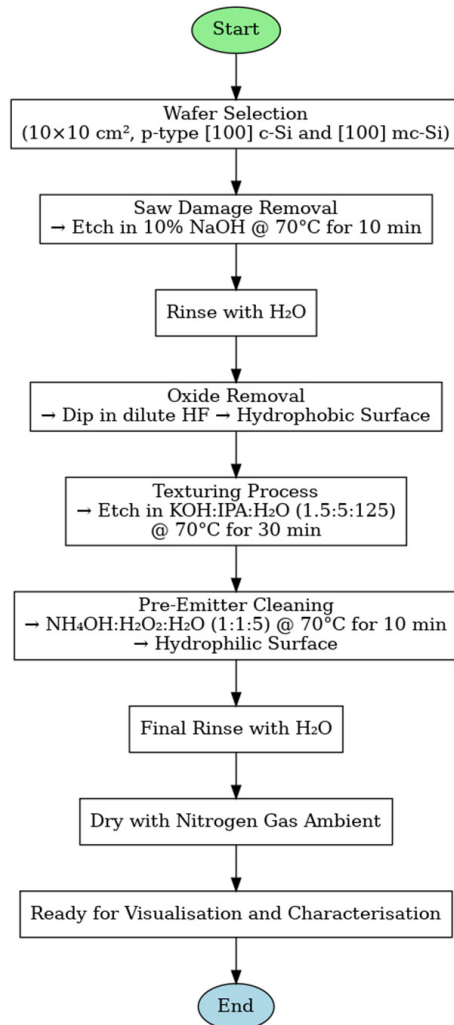


Figure 1: Wafer cleaning and texturing p-rocess flowchart.

After the experiment, scanning electron miscoscopy (SEM) was employed to observed the surface morphology of c-Si and mc-Si samples, highlighting surface morphology and texturing. This procedure will be evaluate the condition of Si wafers before and after the cleaning process with nitric/HF etching. Other than that, Energy-dispersive X-ray (EDX) analysis was performed to identify elemental composition and detect any surface impurities or treatment elements. The EDX evaluation will be before and after the damage removal process on Si wafers with nitric/HF etching. In addition, area roughness was also evaluated through SEM image analysis to compare surface topography for as-cut c-Si, c-Si after damage removal, c-Si with pyramid textured and

mc-Si. Generally, c-Si should exhibit smoother surfaces, while poly-Si show higher surface roughness due to grain structures. Roughness parameters such as average roughness (R_a) provided insights into surface uniformity, influencing light scattering and potential solar cell performance.

2. RESULTS AND DISCUSSION

Figure 2 displays SEM analysis on the c-Si wafer before cleaning. Si wafers are fundamental components in semiconductor device fabrication, serving as substrates for integrated circuits and other electronic devices. The surface morphology of Si wafers before any cleaning or damage removal processes is a critical factor in determining the quality and performance of the final devices. Si wafers are typically sliced from a single-crystal Si ingot using a diamond wire saw or a laser cutting technique. This slicing process can introduce micro-roughness and surface texture variations at the micro or nanoscale, as illustrated in Figure 2. However, micro-roughness can affect the uniformity of thin films deposited during later fabrication steps, influencing device performance. Hence, surface texture analysis often reveals microscopic grooves and ridges (formed during the slicing process) but also produces step-terraces (resulting from the crystallographic orientation of the Si).

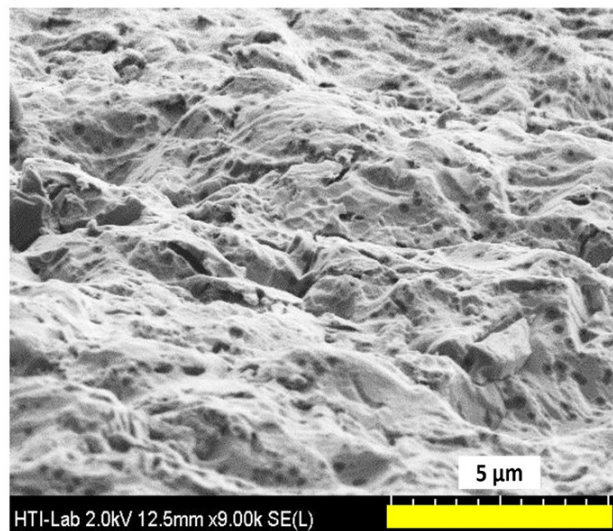


Figure 2: SEM pictures analysis on c-Si before the cleaning process.

All elements on the Si wafer surface are identified using an EDX, as in Figure 3. Surface contaminants on Si wafers can originate from various sources during manufacturing and handling. These contaminants can significantly affect the

performance and reliability of semiconductor devices. The EDX analysis of the as-cut Si wafer is displayed in Figure 3. The element prominent in the EDX scan is Si (86.38%), with low quantities of carbon (C) (7.40%), oxygen (O) (2.96%), nitrogen (N) (2.44%), fluorine (F) (0.43%) and iron (Fe) (0.39%). Metals such as Fe, copper (Cu) and aluminum (Al) can be deposited on the wafer surface through contact with processing equipment and tools. These metallic contaminants can introduce deep-level traps in the Si, affecting the electrical properties of the devices. Despite this, Fe precipitates can cause severe efficiency degradation in solar cells when exposed to moisture, O, heat, light, mechanical stress and reverse bias.^{33–36} Other than that, when Si wafers are exposed to air, they naturally form a thin layer of silicon dioxide (SiO_2) on their surface. This native oxide layer can vary in thickness (typically a few nano-meters) and is often uneven. Accordingly, the presence of this oxide layer can influence the electrical characteristics of the wafer, and its removal is usually necessary before further processing. In addition, oxide precipitates during solar cell production can cause severe efficiency degradation, limiting the lifetime of Si solar cell wafers.^{33,37–39} The surface morphology of Si wafers before cleaning and damage removal encompasses various imperfections and contaminants that can significantly influence semiconductor device fabrication. Thus, the cleaning and damage process on Si wafers should be performed prior to fabricating Si solar cells by minimising the various imperfections and contaminants, as depicted in Figure 2 and Figure 4 on c-Si, to gain higher overall performance.

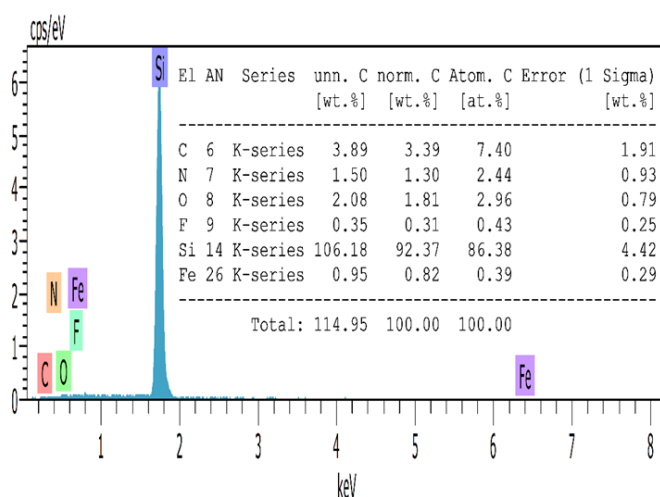


Figure 3: EDX scan and contamination table of the as-cut surface with Fe and other minants; C concentration is system-dependent.

Figure 4 displays SEM analysis on the mc-Si wafer before it is immersed in a damage-removal solution. Furthermore, mc-Si wafers are widely used in the photovoltaic (PV) industry to produce solar cells. Unlike c-Si, which is grown as a single crystal,

mc-Si consists of multiple crystal grains. This mc-Si structure introduces unique surface morphology characteristics crucial to understanding and improving solar cell efficiency and manufacturing processes. The initial surface of mc-Si wafers is typically rougher compared to c-Si due to the varied orientations of the crystal grains. Similar to c-Si, as portrayed in Figure 2, mc-Si wafers can have various contaminants on their surface before cleaning, such as particulate and metallic contaminants. Particulate contaminants from dust particles, slicing debris, and residues from handling can be present, as illustrated in Figure 4. These particles can create localised defects and affect subsequent processing steps. Meanwhile, metallic contaminants are metals from processing equipment and tools that can be deposited on the wafer surface, potentially causing electronic defects in solar cells. According to Figure 5, those particles illustrated in Figure 4 are classified as contaminants of F, with a high O concentration owing to native oxide, N and C from the Si wafer production process. These contamination of F (0.22%), O (2.41%), N (2.94%) and C (9.38%) have a significant impact on the overall fabrication process and percentage conversion efficiency (PCE) of Si solar cell devices. Contaminants like C, O, N, F and Fe introduce challenges that can degrade solar cell performance. In particular, C and O residues may affect the uniformity of coatings and increase surface reflection losses, reducing light absorption. Meanwhile, N and F residues, although sometimes beneficial, must be carefully controlled to prevent defect formation. F contamination on Si wafers can thin spin-on dielectric films and affect their wetting properties in semiconductor manufacturing.^{40–42}

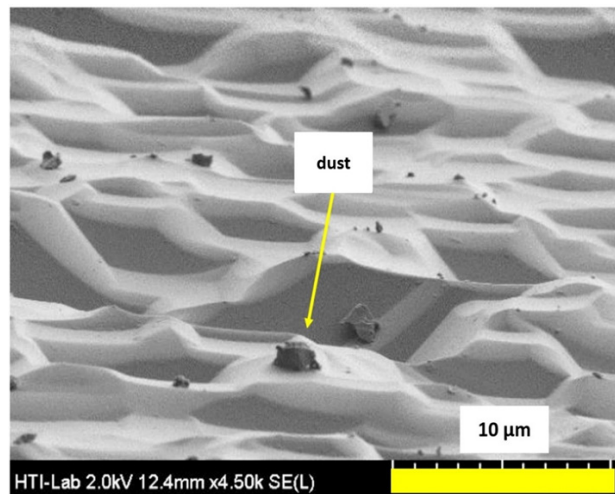


Figure 4: The SEMS before the damage removal process on mc-Si wafers with nitric/HF etching.

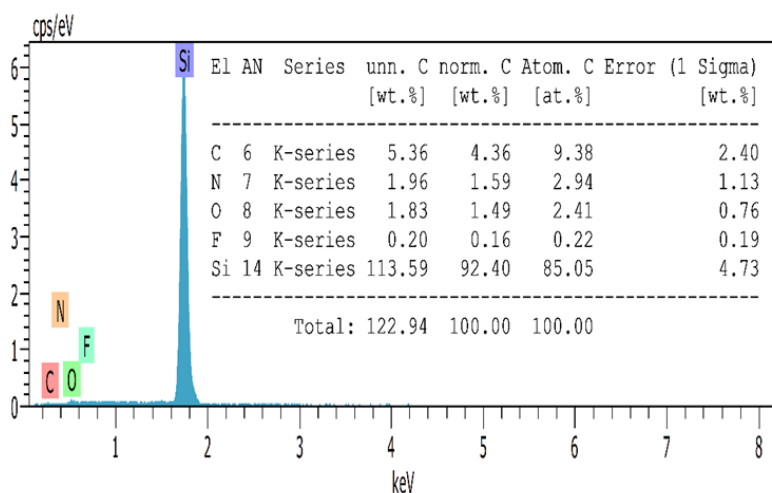


Figure 5: EDX scan before the damage removal process on mc-Si wafers with nitric/HF etching.

In order to eliminate both particulate contaminants and metallic contaminants, cleaning and damage removal processes on mc-Si have been conducted. Figure 6 displays an mc-Si wafer after cleaning and damage removal processes using an acidic solution to remove all the residue and dust. This wet-chemical etching procedure is used to etch the mc-Si substrate to a thickness of around $\sim 5\ \mu\text{m}$ – $12\ \mu\text{m}$ thick. Compared with Figure 4, the surface of the mc-Si wafer displayed in Figure 6 is almost free from contamination and has a much smoother surface. The cleaning process on the Si wafer will successfully remove or reduce contaminations.^{1,2,43–46} Meanwhile, the damage removal process on Si wafers is a critical step for excellent passivation on Si wafers that will enhance solar cell performance.^{25,47,48} After the cleaning and damage removal processes, the surface morphology of mc-Si wafers undergoes significant changes. These processes are essential to prepare the wafers for further semiconductor fabrication steps, such as doping, deposition and etching, which are crucial for producing efficient solar cells and other electronic devices. Compared with EDX data in Figure 5, the percentage of Si increases from 85.08% to 90.8%. At the same time, F and N contaminants are eliminated after the damage removal process with nitric/HF etching. In addition, there is a significant reduction in the contamination percentage by C (9.38%–7.50%) and O (2.41%–1.70%), as depicted in EDX from Figure 7. Thus, the damage removal process using nitric/HF etching on mc-Si effectively eliminates and reduces the contamination after the Si wafers production process.

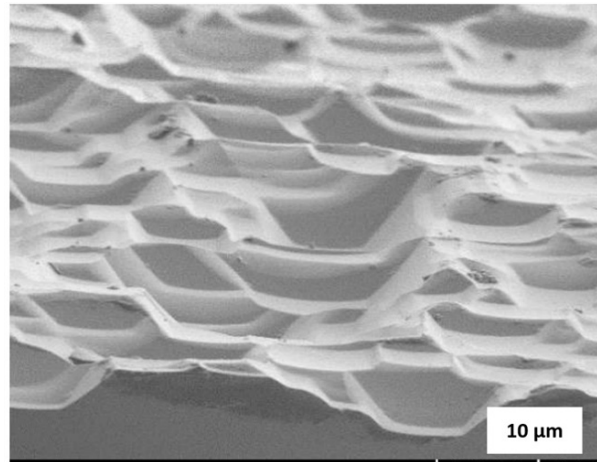


Figure 6: The SEM after the damage removal process on mc-Si wafers with nitric/HF etching.

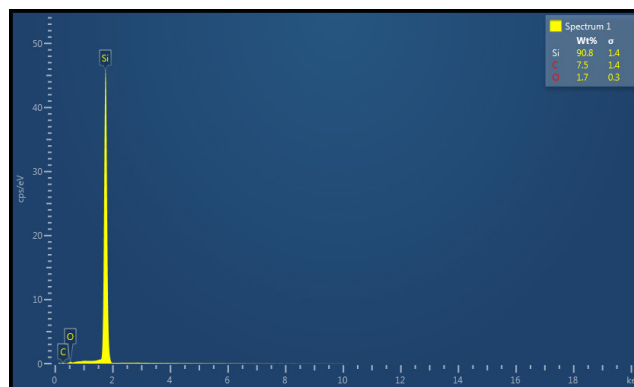


Figure 7: EDX scan along with the contamination table following the nitric/HF treatment.

After being etched, Figure 7 displays the element composition and concentration on the wafer surface. The cleaning and damage removal process using nitric/HF etching significantly improves the surface morphology of mc-Si wafers by effectively reducing both particle and metallic contaminants. Prior to cleaning, wafers typically exhibit numerous particulate contaminants from environmental dust, slicing residues, handling and metallic contaminants such as Fe, oxides, C, N and F from equipment contact and environmental exposure, as illustrated in Figure 3. These contaminants negatively impact device performance by causing localised defects, non-uniform film deposition, etching irregularities and introducing deep-level traps that affect electrical properties. Meanwhile, post-cleaning, the nitric/HF etching process, which combines the oxidising action of HNO_3 with the etching capabilities of HF, drastically reduces particle contaminants by over 90%. It also lowers metallic contaminant

concentrations by several orders of magnitude, which is displayed in Figure 7. This results in a smoother, cleaner surface with fewer visible defects and improved electrical properties, such as lower leakage currents and higher carrier lifetimes, compared with Figure 4. Note that characterisation techniques like SEMS and EDX confirm these improvements, highlighting significantly fewer contaminants and a more uniform surface. This enhances the efficiency and reliability of solar cells and other semiconductor devices.

After the cleaning procedure, the Si surfaces appear bright, clean, smooth and hydrophobic, as displayed in Figure 8(a). Previous research suggested optimising light trapping in solar cells, with typical pyramid textures needing to be developed through wet-chemical etching using a chemical bath alkaline solution for both sides.^{49–56} The Si wafer follows a texturisation process with alkaline-wet chemical etching, as displayed in Figure 8(b). Due to the texturing technique, the surface appears rough, gloomy and dark. The picture of the mc-Si wafer is illustrated in Figure 8(c). The mc-Si is readily visible in the photograph, consisting of numerous crystals randomly positioned throughout the wafer surface.

According to Figure 8(a), the damage removal and cleaning processes significantly improve the condition and morphology of both as-cut and polished c-Si wafers. Initially rough with micro-cracks and saw marks, as-cut wafers become smoother and more uniform after chemical etching and cleaning, though they still retain some residual roughness and defects. Notably, these processes also effectively reduce contaminants introduced during cutting. In contrast, polished wafers, which start with a mirror-like finish and minimal defects due to mechanical and chemical polishing, maintain their smooth, uniform surface post-cleaning, with any minor polishing-induced defects further minimised. Furthermore, the cleaning process ensures that both wafer types achieve the necessary surface quality for subsequent semiconductor processing, with polished wafers exhibiting exceptionally low roughness, minimal defects and low contaminant levels, making them ideal for high-precision applications. Overall, cleaning and damage removal can eliminate contaminations and surface defects that will enhance the photo-electrical performance of Si solar cells.^{47, 48, 57}

After the texturing process, as displayed in Figure 8(b) and Figure 8(c), the condition and morphology of c-Si wafer surfaces, enhanced by alkaline-wet chemical etching, exhibit significant improvements crucial for solar cell efficiency. The etching, typically using KOH or NaOH with additives like IPA, creates uniform pyramid-like structures that increase surface roughness and enhance light trapping by reducing reflectance. Note that these pyramidal structures result from the anisotropic etching properties of the alkaline solution. It etches Si at varying rates along various crystallographic planes, typically exposing the [111] planes. Moreover, this process also minimises surface defects and effectively removes contaminants, ensuring a cleaner wafer surface.

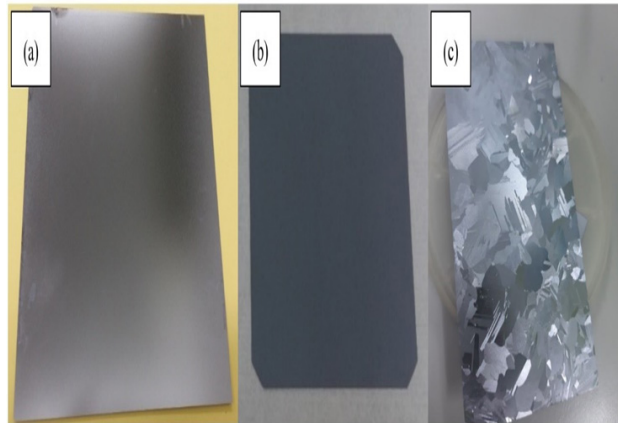


Figure 8: Shows (a) front view of a c-Si wafer after the damage reduction process, (b) alkaline-wet chemical etching was utilised after the texturing process and (c) after texturing, a mc-Si wafer.

The IPA solution used in the texturing process impacts the size of the pyramid, as displayed in Figure 9(a). The pyramid's structure becomes more uniform with the presence of IPA at an optimal concentration. The IPA solution used in the texturing process impacts the size of the pyramid texture on Si surfaces. As such, the pyramid texture on the wafer surface becomes more uniform with the presence of IPA solution at the optimal concentration.

In addition, previous research has explained that anisotropic chemical etching of Si [100] crystal-oriented wafers gives rise to textured surfaces.^{24,58–63} The characteristics of the etching depend upon the time of etching rate, temperature components of the solution and concentration. However, with a dilute NaOH solution that contains IPA and DI water, the Si with [100] crystal-orientation smooth wafers can grow pyramidal surface texture at 70°C temperature. In particular, the surface texturing was performed by asymmetric etching the wafers' front surface using a dilute alkaline solution. The loss in mass of each wafer is estimated from the mass of the wafer measured with a microbalance before and after texturing, which subsequently leads to the estimation of the etched thickness of the wafer and, hence, the etch rate.

Other than that, Figure 9(b) exhibits surface texturisation by an alkaline solution on the surface of the mc-Si wafer. After the texturisation process, the morphology on the mc-Si surface demonstrates an almost square-shaped crater. Thus, these structures are much more different from the textured morphology on c-Si wafers, which is pyramidal textures. In conjunction, the alkaline etchant is more effective in etching [100] Si surfaces and much quicker than [111] mc-Si surfaces. The etching rate of the [111] planes is much slower compared to the [100] or [110] planes. This anisotropic

behaviour indicates that the etching does not proceed uniformly across all directions, forming distinct surface features based on the crystallographic planes exposed during etching. Poly-Si wafers have many small crystallites or grains, each with different orientations. When an alkaline solution like NaOH or KOH etches these grains, the planes are etched at different rates—however, the square-shaped craters formed by this texturing process benefit light trapping. The rough, cratered surface scatters incoming light, increasing the absorption of sunlight and improving the efficiency of the solar cell. Moreover, overly deep craters could lead to surface defects or increased recombination losses, so the process must be carefully controlled.

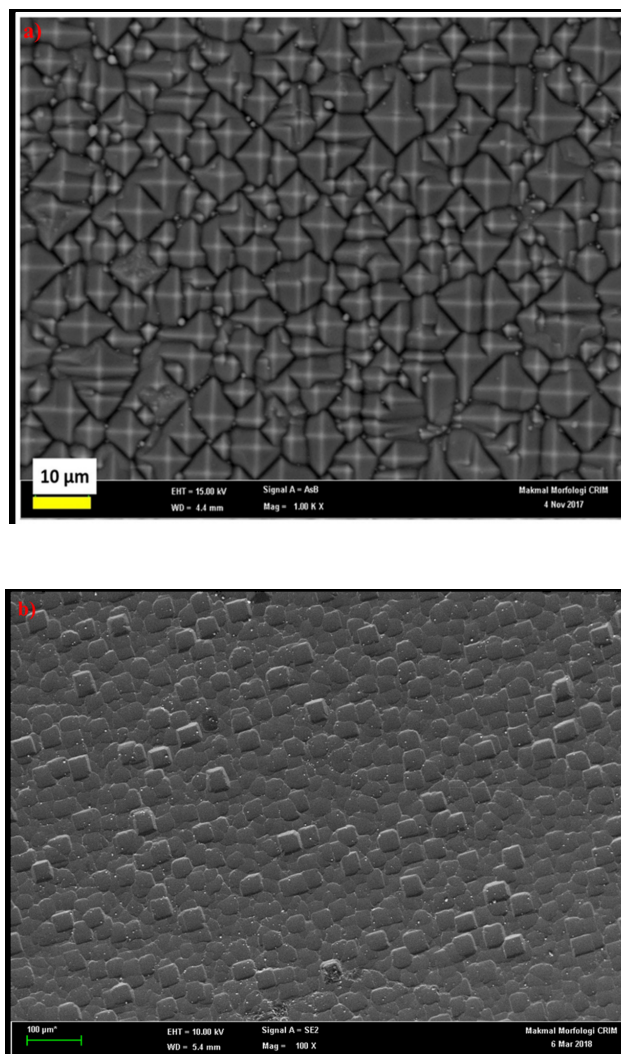


Figure 9: FESEM evaluation of alkaline etching on (a) c-Si and (b) mc-Si.

Figure 10 displays a close view of the pyramidal texture by alkaline etchant on c-Si wafers. The textured size is approximately $6\text{ }\mu\text{m}$ – $9\text{ }\mu\text{m}$ in height and $6\text{ }\mu\text{m}$ in width, as illustrated in Figure 10. Meanwhile, the base angle of the pyramid is in the range of 54.00° – 54.50° . According to the findings, at a temperature of 70°C – 80°C , it is possible to construct an ideal pyramid shape all over the wafer surface. The base angle of the pyramid textured presented here is about 54.00° – 55.00° . Alternatively, Omar et al. reported that the base angle of the texture should be close to 50.00° – 52.00° and most commonly accepted 54.74° .¹⁶

On the other hand, Rais et al. described from the PC3S simulation analysis of spectral transmission in Si solar cell with pyramidal texturisation: the front surface was higher than under the practical and proposed base angles of texture around 50° – 52° .⁷ Balaji et al. mentioned that for a (100) crystal orientation Si wafer, a solution of NaOH, IPA and DI water creates square-based four-sided pyramids consisting of sections of [111] planes which form internal angles of 54.7° with the (100) crystal orientation surface.⁶⁴

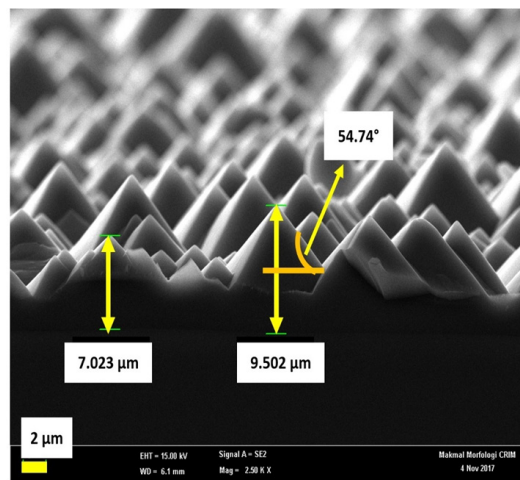


Figure 10: Wafer cross-section, with an average of roughly $8\text{ }\mu\text{m}$.

The data in Table 2 provides insights into the surface roughness and topography of different Si wafers after various treatments, including as-cut, damage removal, pyramid texturing and mc-Si samples. These metrics—area roughness and root mean square (RMS) roughness—are critical in determining the suitability of wafers for PV applications, where surface morphology impacts both electrical performance and light absorption efficiency. The as-cut c-Si wafer exhibits an area roughness of 60.28 nm and RMS roughness of 77.41 nm , reflecting surface damage and mechanical

irregularities introduced by sawing. This initial roughness is relatively high, hindering efficient processing and performance and necessitating damage removal to improve surface quality.

After damage removal, the c-Si wafer exhibits a significant reduction in roughness, with area roughness decreasing to 37.56 nm and RMS roughness to 32.74 nm. This smoother surface indicates the effective elimination of surface defects and residual stress, preparing the wafer for further processing steps such as texturisation. Meanwhile, the pyramid-textured c-Si wafer has an area roughness of 99.08 nm and RMS roughness of 77.97 nm. The increase in roughness compared to the damage-removed wafer is intentional, as the textured surface enhances light trapping and absorption, which are essential for improving solar cell efficiency.

In contrast, the mc-Si wafer presents the highest roughness values, with an area roughness of 179.34 nm and RMS roughness of 272.13 nm. This elevated roughness is attributed to the presence of grain boundaries and multiple crystal orientations, which introduce surface irregularities. Although higher roughness can promote light scattering, it may also increase recombination losses, potentially affecting the electrical performance of solar cells. The surface treatments reflect a trade-off between smoothness and roughness, depending on the intended purpose. While smoother surfaces enhance electrical properties, textured surfaces like pyramid structures are necessary to optimise light absorption. Despite its roughness, the mc-Si wafer can still be beneficial in applications where light scattering is advantageous. According to these research, by minimising surface stains and impurities, enhancing surface texturing and passivation and optimising electrical and optical characteristics, cleaning and damage removal of silicon wafers can improve the overall performance of solar cells.^{24,48,65–70} Thus, proper wafer surface treatment plays a vital role in boosting solar cell efficiency. By eliminating contaminants and surface defects, it enables better light absorption and carrier collection. These enhancements highlight the crucial impact of surface preparation on the overall functionality and performance of photovoltaic devices.

Table 2: Damage removal (DR), textured pyramidal structure, polycrystalline wafer topography, area roughness and RMS of as-cut.

Sample	Area roughness (nm)	RMS
As-cut c-Si	60.28	77.41
c-Si (Damage removal)	37.56	32.74
c-Si (Pyramid textured)	99.08	77.97
mc-Si	179.34	272.13

3. CONCLUSION

The cleaning and damage removal processes on c-Si and mc-Si are vital in preparing these substrates for further fabrication. Furthermore, SEM and EDX analyses confirm that the presence of surface contaminants, such as C, O, N and Fe, can negatively impact electrical properties and performance. At the same time, the nitric/HF etching process effectively eliminates these contaminants, yielding smoother surfaces with improved Si content. In addition, wet-chemical etching with alkaline solutions produces textured surfaces on mc-Si wafers, enhancing light trapping and minimising reflectance. Accordingly, these processes reduce surface defects, improve electrical properties and ensure that the wafers meet the quality requirements for high-efficiency solar cells and reliable semiconductor devices. In conclusion, meticulous cleaning, damage removal and surface texturisation are crucial to achieving superior wafer performance, ultimately contributing to advancements in PV and semiconductor technologies.

4. ACKNOWLEDGEMENTS

This work has been supported by a Universiti Sains Malaysia Short-Term Grant with project number: R501-LR-RND002-0000000210-0000. This work has been conducted with the support and guidance of the Advanced Silicon Solar Cell Fabrication Laboratory, Solar Energy Research Institute (SERI), Universiti Kebangsaan Malaysia. In addition, we would like to express many thanks to Dr. Saleem H. Zaidi from Gratings Incorporated, Albuquerque, New Mexico, USA, for collaboration and guidance in completing the whole process of the theoretical and experimental works.

5. REFERENCES

1. Tsai, T. H. & Wang, C. Y. (2023). A study of ammonium bifluoride as an agent for cleaning silicon contamination in the wafer dicing process. *Appl. Sci.*, 13(9), 5294. <https://doi.org/10.3390/app13095294>
2. Ryu, K. et al. (2023). Dissolution behavior of metal impurities and improvement of reclaimed semiconductor wafer cleaning by addition of chelating agent. *Arch. Metall. Mater.*, 66(4), 977–981. <https://doi.org/10.24425/amm.2021.136409>
3. Yang, S. et al. (2020). Silicon recovery from diamond wire saw silicon powder waste with hydrochloric acid pretreatment: An investigation of Al dissolution behavior. *Waste Manag.*, 120, 820–827. <https://doi.org/10.1016/j.wasman.2020.11.005>
4. Soha, M. et al. (2020). Investigation of ppb-level surface contamination of n-type silicon solar cells. *Appl. Surf. Sci.*, 520, 146299. <https://doi.org/10.1016/j.apsusc.2020.146299>

5. Yim, V. et al. (2023). Development of intentional contamination in iron by bath for silicon wafers and evaluation of VPD-bulk and LPD-bulk for metallic contaminants Analyses by ICPMS. *Solid State Phenom.*, 346, 210–215. <https://doi.org/10.4028/p-ufkqd2>
6. Seo, J. (2020). Chemical mechanical planarization-related to contaminants: Their sources and characteristics. *Emerg. Contam.*, 17. <https://doi.org/10.5772/intechopen.94292>
7. Rais, A. R. M. et al. (2021). Analysis of spectral transmission in Si solar cell with pyramidal texturization by using PC3S simulation. *Silicon*, 14, 8981–8992. <https://doi.org/10.1007/s12633-021-01373-0>
8. Zhang, S. et al. (2020). Spherical-chain silica with super-hydrophobic surface and ultra-low refractive index for multi-functional broadband antireflective coatings. *Sol. Energy*, 207, 1222–1230. <https://doi.org/10.1016/j.solener.2020.05.060>
9. Ma, X. et al. (2020). The optical properties of a visible light filter integrated on the silicon substrate. *Opt. Commun.*, 464, 125510. <https://doi.org/10.1016/j.optcom.2020.125510>
10. Stevens, L. et al. (2021). Impact of the refractive index on coupling structures for silicon solar cells. *J. Photonics Energy*, 11, 1–14. <https://doi.org/10.1117/1.jpe.11.027001>
11. Zambree, A. S. et al. (2023). Modelling and optimization of a light trapping scheme in a silicon solar cell using silicon nitride (SiNx) anti-reflective coating. *Trends Sci.*, 20(9), 5555. <https://doi.org/10.48048/tis.2023.5555>
12. Srivastava, A. et al. (2022). Excellent omnidirectional light trapping properties of inverted micro-pyramid structured silicon by copper catalyzed chemical etching. *Opt. Mater. (Amst.)*, 131, 112677. <https://doi.org/10.1016/j.optmat.2022.112677>
13. Barkhouse, D. A. R. et al. (2015). Yield predictions for photovoltaic power plants: Empirical validation, recent advances and remaining uncertainties. *Prog. Photovoltaics Res. Appl.*, 20, 6–11. <https://doi.org/10.1002/pip.2616>
14. Kim, M. S. et al. (2020). Review: Surface texturing methods for solar cell efficiency enhancement. *Int. J. Precis. Eng. Manuf.*, 21(7), 1389–1398. <https://doi.org/10.1007/s12541-020-00337-5>
15. Narottam, D. et al. (2020). Light reflection loss reduction by nano-structured gratings for highly efficient next-generation GaAs solar cells. *Energies (MDPI)*, 13(16), 4198. <https://doi.org/10.3390/en13164198>
16. Omar, H. D. et al. (2020). Ray tracing of inverted pyramids for light-trapping in thin crystalline silicon for solar cells. *Optik (Stuttg)*, 219, 165279. <https://doi.org/10.1016/j.ijleo.2020.165279>
17. Oni, A. M. et al. (2024). A comprehensive evaluation of solar cell technologies, associated loss mechanisms, and efficiency enhancement strategies for photovoltaic cells. *Energy Reports*, 11, 3345–3366. <https://doi.org/10.1016/j.egyr.2024.03.007>
18. Rais, A. R. M. et al. (2021). Photo-generation profiles in deeply-etched, two-dimensional patterns in interdigitated back contact solar cells. *J. Ovonic Res.*, 17, 283–289. <https://doi.org/10.15251/jor.2021.173.283>
19. Radfar, B. et al. (2020). Effects of different laser modified surface morphologies and post-texturing cleanings on c-Si solar cell performance. *Renew. Energy*, 145, 2707–2714. <https://doi.org/10.1016/j.renene.2019.08.031>

20. Zhu, L. et al. (2022). Ultrafast random-pyramid texturing for efficient monocrystalline silicon solar cells. *Sol. RRL*, 6(7), 2200204. <https://doi.org/10.1002/solr.202200204>
21. Dieye, A. et al. (2022). Impact of texturing silicon coated with a single antireflective layer. *Int. J. Adv. Res.*, 10(9), 222–227. <https://doi.org/10.21474/ijar01/15345>
22. Mercier, T. et al. (2021). High symmetry nano-photonics quasi-crystals providing novel light management in silicon solar cells. *Nano Energy*, 84, 105874. <https://doi.org/10.1016/j.nanoen.2021.105874>
23. Malik, P. et al. (2023). Double layered silicon nitride coated pyramid formation by etching on silicon substrate for photovoltaic application. *Women in Optics and Photonics in India 2022 (SPIE)*, 12638, 126380H-126380H–7, 19. <https://doi.org/10.1117/12.2669974>
24. Jung, Y. et al. (2020). Pre-texturing thermal treatment for saw-damage-removal-free wet texturing of monocrystalline silicon wafers. *Energies*, 13(24), 6610. <https://doi.org/10.3390/en13246610>
25. Jung, Y. et al. (2020). Novel double acidic texturing process for saw-damage-free kerfless multicrystalline silicon wafers. *IEEE J. Photovoltaics*, 10, 1545–1551. <https://doi.org/10.1109/jphotov.2020.3014858>
26. Pu, T. et al. (2020). Temperature effect of nano-structure rebuilding on removal of DWS mc-Si Marks by Ag/Cu MACE process and solar cell. *Energies*, 13(18), 4890. <https://doi.org/10.3390/en13184890>
27. Kim, M. et al. (2020). Study on efficiency improvement of multi-crystalline silicon solar cell by removing by-product and plasma induced damage generated during reactive ion etching. *Curr. Appl. Phys.*, 20, 519–524. <https://doi.org/10.1016/j.cap.2020.01.013>
28. Ullattil, S. et al. (2021). Investigations on the influence of surface textures on optical reflectance of multi-crystalline silicone (mc-Si) crystal surfaces-simulations and experiments. *Int. J. Renew. Energy Dev.*, 11(2), 375–383. <https://doi.org/10.14710/ijred.2022.38538>
29. Jung, Y. et al. (2021). Effective surface texturing of diamond-wire-sawn multicrystalline silicon wafers via crystallization of the native surface amorphous layer. *IEEE J. Photovoltaics*, 11, 43–49. <https://doi.org/10.1109/jphotov.2020.3035122>
30. Jung, Y. et al. (2020). Effective additive-free acidic-solution texturing for surface-damage-free kerfless silicon wafers. *IEEE J. Photovoltaics*, 10, 431–437. <https://doi.org/10.1109/jphotov.2019.2963573>
31. Jung, Y. et al. (2021). 19.2%-Efficient multicrystalline silicon solar cells via additive-free mechanical grinding surface pretreatment for diamond-wire-sawn wafers. *IEEE J. Photovoltaics*, 11, 36–42. <https://doi.org/10.1109/jphotov.2020.3033972>
32. Srivastava, A. et al. (2021). Highly efficient pedot:pss/silicon hybrid solar cells via effective surface microengineering of low-cost solar-grade silicon wafers. *ACS Appl. Energy Mater.*, 4, 4181–4198. <https://doi.org/10.1021/acsaem.1c00511>
33. Dunfield, S. P. et al. (2020). From defects to degradation: A mechanistic understanding of degradation in perovskite solar cell devices and modules. *Adv. Energy Mater.*, 10(26), 1904054. <https://doi.org/10.1002/aenm.201904054>
34. Schubert, M. et al. (2019). Limiting defects in n-type multicrystalline silicon solar cells. *Phys. Status Solidi*, 216(17), 1900331. <https://doi.org/10.1002/pssa.201900331>

35. Hu, Z. et al. (2021). Role of metal impurities in multicrystalline silicon solar cell degradation. *Appl. Phys. Express*, 14(11), 115502. <https://doi.org/10.35848/1882-0786/ac2ae6>
36. Boyd, C. C. et al. (2018). Understanding degradation mechanisms and improving stability of perovskite photovoltaics. *Chem. Rev.*, 119(5), 3418–3451. <https://doi.org/10.1021/acs.chemrev.8b00336>
37. Schön, J. et al. (2021). Experimental and theoretical study of oxygen precipitation and the resulting limitation of silicon solar cell wafers. *IEEE J. Photovoltaics*, 11, 289–297. <https://doi.org/10.1109/jphotov.2020.3044353>
38. Onishi, K. et al. (2018). Evaluation of lifetime degradation caused by oxygen precipitation combined with metal contamination in Cz-Si for solar cells. *2018 IEEE 7th World Conf. Photovolt. Energy Convers. (A Jt. Conf. 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC)*, 360–362. <https://doi.org/10.1109/PVSC.2018.8547349>
39. Weu, A. et al. (2019). Oxygen-induced doping as a degradation mechanism in highly efficient organic solar cells. *ACS Appl. Energy Mater.*, 2(3), 1943–1950. <https://doi.org/10.1021/ACSAEM.8B02049>
40. Kim, H. et al. (2018). Effects of fluorine contamination on spin-on dielectric thickness in semiconductor manufacturing. *Advances in Patterning Materials and Processes XXXV (SPIE)*, 10586, 56. <https://doi.org/10.1117/12.2297309>
41. Garnier, P. & de Buttet, C. (2023). Silicon and germanium corrosion by fluorinated chemistry in presence of wafer charging. *Solid State Phenom.*, 346, 63–68. <https://doi.org/10.4028/p-ysmbh5>
42. Hsieh, W. et al. (2019). The probe marker discoloration on Al pad and wafer storage. *2019 IEEE 26th Int. Symp. Phys. Fail. Anal. Integr. Circuits*, 1–4. <https://doi.org/10.1109/IPFA47161.2019.8984909>
43. Zhao, Q. et al. (2022). Control of the micro-defects on the surface of silicon wafer in chemical mechanical polishing. *ECS J. Solid State Sci. Technol.*, 11(2), 023009. <https://doi.org/10.1149/2162-8777/ac546d>
44. Wang, C. et al. (2018). Low-temperature wafer direct bonding of silicon and quartz glass by a two-step wet chemical surface cleaning. *Jpn. J. Appl. Phys.*, 57, 02BD02. <https://doi.org/10.7567/jjap.57.02bd02>
45. Li, K. et al. (2022). Mechanism analysis of megasonic and brush cleaning processes for silicon substrate after chemical mechanical polishing. *ECS J. Solid State Sci. Technol.*, 11(10), 104004. <https://doi.org/10.1149/2162-8777/ac9c2e>
46. Matsuo, M. et al. (2020). Side wall water outlet design for silicon wafer wet cleaning bath. *Mater. Sci. Semicond. Process.*, 110, 104970. <https://doi.org/10.1016/j.mssp.2020.104970>
47. Nsofor, U. et al. (2018). Analysis of silicon wafer surface preparation for heterojunction solar cells using X-ray photoelectron spectroscopy and effective minority carrier lifetime. *Sol. Energy Mater. Sol. Cells*, 183, 205–210. <https://doi.org/10.1016/j.SOLMAT.2018.03.006>
48. Li, X. et al. (2020). Improvement of saw damage removal to fabricate uniform black silicon nanostructure on large-area multi-crystalline silicon wafers. *Sol. Energy*, 204, 577–584. <https://doi.org/10.1016/j.solener.2020.03.072>

49. Hohn, O. et al. (2017). Impact of front side pyramid size on the light trapping performance of wafer based silicon solar cells and modules. *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)*, 352–355. <https://doi.org/10.1109/pvsc.2017.8366607>
50. Mandel, S. (2020). Pyramid texturing on silicon solar cells traps light more efficiently. *Scilight*, 2020(7), 71106. <https://doi.org/10.1063/10.0000805>
51. Subhan, F. et al. (2020). Optical optimization of double-side-textured monolithic perovskite–silicon tandem solar cells for improved light management. *RSC Adv.*, 10, 26631–26638. <https://doi.org/10.1039/d0ra04634e>
52. Xu, Z. et al. (2020). Optical functional film with triangular pyramidal texture for Crystalline silicon solar cells. *Sol. Energy*, 201, 45–54. <https://doi.org/10.1016/j.solener.2020.02.081>
53. Li, Y. et al. (2022). Nanopyramid texture formation by one-step ag-assisted solution process for high-efficiency monocrystalline Si solar cells. *Sol. RRL*, 6(11), 2200707. <https://doi.org/10.1002/solr.202200707>
54. Gao, K. et al. (2021). Inverted pyramid morphology control by acid modification and application for perovskite solar cells. *ACS Omega*, 6, 32925–32929. <https://doi.org/10.1021/acsomega.1c04972>
55. Wang, J. et al. (2021). Improvement of bifacial heterojunction silicon solar cells with light-trapping asymmetrical bifacial structures. *Sol. Energy*, 223, 229–237. <https://doi.org/10.1016/j.solener.2021.05.041>
56. Dai, R. et al. (2022). Improved interfacial contact for pyramidal texturing of silicon heterojunction solar cells. *molecules*, 27(5), 1710. <https://doi.org/10.3390/molecules27051710>
57. Sun, L. et al. (2022). Towards investigating surface quality of single-crystal silicon optics polished with different processes. *Coatings*, 12(2), 158. <https://doi.org/10.3390/coatings12020158>
58. Kashyap, J. et al. (2022). Surface texturisation for the reduction of light reflection in ZnO/Si heterojunction. *Int. J. Sustain. Energy*, 41, 1399–1407. <https://doi.org/10.1080/14786451.2022.2052292>
59. Arafat, M. Y. et al. (2021). Study of black silicon wafer through wet chemical etching for parametric optimization in enhancing solar cell performance by PC1D numerical simulation. *Crystals*, 11(8), 881. <https://doi.org/10.3390/cryst11080881>
60. Altunsoy, B. et al. (2021). Single step inverted pyramid texturing of n-type silicon by copper assisted chemical etching. *2021 IEEE 48th Photovolt. Spec. Conf.*, 1631–1637. <https://doi.org/10.1109/PVSC43889.2021.9518639>
61. Kaffle, B. et al. (2020). On the formation of black silicon features by plasma-less etching of silicon in molecular fluorine gas. *Nanomaterials*, 10(11), 2214. <https://doi.org/10.3390/nano10112214>
62. Kirchner, R. et al. (2020). Anisotropic etching of pyramidal silica reliefs with metal masks and hydrofluoric acid. *Small*, 16(43), 2002290. <https://doi.org/10.1002/sml.202002290>
63. Guo, W. et al. (2020). A study on the damage layer removal of single-crystal silicon wafer after atmospheric-pressure plasma etching. *J. Micro Nano-Manufacturing*, 8(2), 24501. <https://doi.org/10.1115/1.4046377>

64. Balaji, N. et al. (2015). Laser fired local back contact c-Si solar cells using phosphoric acid for back surface field. *J. Electron. Mater.*, 44, 1181–1186. <https://doi.org/10.1007/s11664-015-3652-5>
65. Kashkoush, I. et al. (2014). Wafer surface preparation for high-efficiency solar cells. *2014 IEEE 40th Photovolt. Spec. Conf.*, 1211–1213. <https://doi.org/10.1109/PVSC.2014.6925132>
66. Qinqin, W. et al. (2020). Study on the cleaning process of n+-poly-Si wraparound removal of TOPCon solar cells. *Sol. Energy*, 211, 324–335. <https://doi.org/10.1016/j.solener.2020.09.028>
67. Liu, J. et al. (2024). UV-OZONE treatment for suppressing surface damages on silicon solar cells. *ACS Appl. Mater. Interfaces*, 16(36), 48660–48666. <https://doi.org/10.1021/acsami.4c11246>
68. Choi, J. et al. (2020). Development of eco-friendly cleaning solution for industrial silicon wafer solar cell. *Mater. Sci. Semicond. Process.*, 106, 104764. <https://doi.org/10.1016/j.mssp.2019.104764>
69. Kasim, A. W. (2024). Investigate the electrical and structural characteristics of the Si-ZnO diode. *J. Phys. Sci.* 35, 13–20. <https://doi.org/10.21315/jps2024.35.1.2>
70. Rujhan, A. et al. (2024). Phosphorus activation via screen printing Ag/P on thermally grown SiO₂ layer as passivating contact on n-Si. *J. Phys. Sci.* 35, 65–80. <https://doi.org/10.21315/jps2024.35.3.5>